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(54) **Bias control circuit for an RF power amplifier**

Vorspannungssteuerschaltung eines HF-Leistungsverstärkers

Circuit de contrôle de la polarisation d'un amplificateur RF de puissance

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EP 0 734 118 B1

Description

[0001] The present invention relates to RF amplifiers for mobile telephone communication systems and more particularly to a biasing circuit to provide linear operation of an RF mobile telephone power amplifier.

[0002] References that relate generally to biasing or controlling amplifiers in radio telephone apparatus are as follows.

[0003] In U.S. Patent 5,060,294 issued October 22, 1991 to Schwent et al. and entitled DUAL MODE POWER AMPLIFIER FOR RADIO TELEPHONE, a transmission system is described wherein radio communication signals are both analog mode which are frequency modulated and discrete mode which are composite modulated as a combination of amplitude and phase modulation. In the Schwent et al. patent an amplifier is taught which may be alternately operated in the linear mode for the composite modulation and the saturation mode for the frequency modulation. A switch is provided which is connected to the amplifier to operate it in the linear or the saturation mode.

[0004] In U.S. Patent 4,924,191 issued May 8, 1990 to Erb et al. entitled AMPLIFIER HAVING DIGITAL BIAS CONTROL APPARATUS an amplifier is described that includes a digital bias control apparatus to provide dynamic control over the operating point of a plurality of amplifying elements in the amplifier. A processor is provided to optimize the operating point of each amplifying element as a function of the amplifying element characteristics.

[0005] In U.S. Patent 4,257,009 issued March 17, 1981 to Yorkanis entitled INHIBIT CIRCUIT FOR A DIFFERENTIAL AMPLIFIER a system is described including a pair of non-additive combiners (mixers) connected at their respective outputs to the inverting, and non-inverting, inputs of differential amplifier. A bias controller having an input for receiving a control signal produces a fixed bias voltage at a first output thereof. A conductor is connected to apply the variable bias voltage at the second output to the first inputs of non-additive combiners. A resistor is connected to apply the fixed bias voltage at the first output of the bias controller to a second input of the combiner.

[0006] U.S. Patent 4,901,032 issued February 13, 1990 to Komiak relates to a digitally controlled variable power amplifier for radio frequency signals for driving the individual elements of a phased array radar system in which accurate tapering of the power supplied to individual antenna elements is desired for sidelobe control. The power amplifier must maintain a stable phase transfer response and should remain at a high power transfer efficiency at each reduced power setting. This performance is achieved by the use of power transistor of a segmented dual gate design. The segments of the second gate electrode are of digitally scaled widths and are individually energized to activate digitally scale regions of the transistor. These regions are operated in a saturated class "A" mode in all power settings to achieve the desired stable phase transfer response and high power added efficiency.

[0007] U.S. Patent 4,034,308 issued July 5, 1977 to Wermuth et al. entitled AMPLIFIER WITH CONTROLLABLE TRANSMISSION FACTOR AND SWITCHABLE CONTROL CHARACTERISTICS discloses an amplifier circuit whose gain bears a desired relation to a control voltage, including a differential amplifier, a plurality of impedances interconnected between the amplifier terminals and switches interconnected with the impedances and switchable between two states which create two impedance configurations that give the circuit mutually complementary gain vs. control voltage control characteristics.

[0008] U.S. Patent 5,121,081 issued June 9, 1992 to Hori entitled OUTPUT WAVEFORM CONTROL CIRCUIT discloses an output waveform control circuit for a time division multiple access system including driving circuit which sends a control signal to a power amplifier in accordance with a signal outputted by a comparator circuit. By controlling the operating voltage of the power amplifier simultaneously with the control of the level input signal from the input level control circuit, the output characteristic of the power amplifier, including a class C or the like amplifier having a non-linear input/ output characteristic, is prevented from varying abruptly and the output waveform of the power amplifier is so controlled as to have gently sloped leading and trailing edges.

[0009] In Japanese Patent Publication S54(1979) 104760 dated August 17, 1979 by Hikari Hond and entitled A LOW POWER CONSUMPTION TYPE AMPLIFIER a low power consumption type amplifier is described that is provided with an amplifier circuit which amplifies a specified wideband signal, a signal level detector circuit which detects the signal level of this amplifier circuit and a variable-impedance circuit where the impedance is varied and controlled by means of the output of the said signal level detector circuit and which, by way of the said impedance, supplies power of a specified voltage to the aforementioned amplifier circuit, thereby controlling the said variable-voltage to the aforementioned amplifier circuit, thereby controlling the said variable-impedance circuit so that the aforementioned impedance is caused to be small when the aforementioned signal level is high, and high when the signal level is low.

[0010] GB Patent 2269716 published August 3, 1992, issued to Texas Instruments Limited and entitled SWITCHABLE BIAS CIRCUIT describes a bias circuit for a multistage amplifier that is suitable for use in a cellular telephone or pager. The circuit is capable of both Class A and Class C operation, allowing one or more amplifier stages to switch between high-linearity and high-efficiency regimes. A reference voltage is produced by a first sub-circuit, which comprises a resistor in series with two or more diodes. The bias point of the

amplifier stage depends on the reference voltage, resulting in Class C operation, unless a voltage is applied to a second sub-circuit, causing the amplifier to be biased in Class A.

[0011] The invention provides an RF amplifier circuit comprising a power amplifier stage containing a power transistor, a voltage source and biasing means for providing linear operation of said amplifier circuit, where said biasing means comprises a first resistor means, which is connected in series with a diode, and a current generator circuit coupled to a first node, for generating a current, characterised in that the diode is a transistor, its emitter electrode being coupled to said voltage source and its base and collector electrodes being connected together and coupled through the first resistor means to the first node, a bias control transistor is provided, its collector electrode being coupled to the control electrode of the power transistor, its emitter electrode being coupled to one of the main current conducting electrodes of the power transistor and its base electrode being coupled to the first node so that the bias control transistor is responsive to the voltage at first node and provides a bias control current signal to said power transistor, and a current-to-voltage converter means is connected between the emitter electrode of said bias control transistor and said voltage source; wherein the base-to-emitter voltages of said transistor diode and said bias control transistor are determined by the generated current to be substantially equal, the transistor diode and bias control transistor being identical transistors maintained at equal temperatures.

[0012] Other and further features, and potential advantages and benefits of the invention will become apparent in the following description taken in conjunction with the following drawings. It is to be understood that the foregoing general description and the following detailed description are exemplary and explanatory but are not to be restrictive of the invention.

[0013] The present invention will now be described by way of example by reference to the accompanying drawings, in which:

Figs. 1, 2 and 3 are schematic illustrations of known circuits for RF power amplifier bias control; and

Fig. 4 is a schematic circuit illustration of an RF power amplifier structure having a bias control circuit according to the principles of the present invention.

[0014] Like numerals refer to like parts throughout the disclosure.

[0015] With digitally modulated signals (such as by phase-shift keying etc.) a linear power amplifier is needed. Usually with analog mobile phones RF-power amplifiers are biased in class C. This means that an incoming RF-signal is needed in order to make the transistor in the amplifier conduct. This technique is simple, but with signals containing AM-modulation a marked distortion occurs. In order to keep the distortion low the RF-stages have to be biased to a current level sufficient that the needed RF-power can be achieved with low distortion. Bipolar transistors have quite large variation in DC current gain (hfe). To get the amplifier stage biased at the desired current without too high of a voltage drop in the DC feedback circuit (collector resistor) an active biasing circuit is needed. Typically a PNP transistor is used in the feedback circuit of the amplifier stage The PNP transistor controls the base current of the RF-transistor so that the voltage drop over the RF-transistor's collector resistor equals the voltage (Vbat-Vbpnp)-Vbepnp where Vbpnp is the voltage at the base of the PNP transistor and Vbepnp is the base emitter voltage of the PNP transistor. If a low voltage drop is needed, the temperature dependence of Vbepnp makes the biasing circuit dependent on temperature. To avoid this, temperature compensation is needed. Temperature compensation may be accomplished with a pnp transistor connected as a diode. With these circuit techniques it is possible to bias the RF-power amplifier into linear operation. Cellular phones use several power levels, so if the power amplifier is biased for the highest power level, the efficiency with lower power levels is very low.

[0016] Typical known techniques for RF power amplifier bias control are illustrated in Figs. 1, 2 and 3.

[0017] Referring to Fig. 1, a bias control stage using bi-polar technology is shown including a voltage regulator supply Vreg and a DC voltage supply Vbat. A trimmer resistor 10 is tuned until transistor 12 has reached an optimum current for the desired operation. A diode 14 is used to compensate the temperature dependence of the transistor 12. To tune the circuit of Fig. 1 for a number of different power levels that may be employed in actual operation of the circuit, different power levels of Vreg can be provided, such as from a digital-to-analog converter, and the circuit is tuned for each power level during the manufacture of the circuit. Each of the values of current are stored in a read-only memory. If later, the transistor 12 has to be changed, the tuning would have to be done again.

[0018] Fig. 2 illustrates a bias control circuit similar to that of Fig. 1 but using a GaAsFET device 16 instead of bipolar device 12. The circuit of Fig. 2 uses the same tuning procedures and includes the same temperature compensation as Fig. 1.

[0019] The drawbacks with the techniques of Figs. 1 and 2 are that the biasing needs tuning during circuit manufacture and if the power transistor is later changed, new tuning is needed. Also, the temperature compensation is difficult, particularly for the bipolar stage.

[0020] For low signal RF amplifiers, an active bias circuit is often employed. A typical active bias circuit is illustrated in Fig. 3.

[0021] In Fig. 3, a resistive divider composed of resistors 20 and 22 provides a base voltage Vb at node 24 to transistor 26. The emitter 28 of transistor 26 is connected to the low voltage end of resistor 30. Transistor

26 controls the bias current (the base current) of transistor 32 in such a manner that the voltage at the emitter 28 of transistor 26 is a base-emitter voltage (Vbe) higher than Vb (that is, Vb & Vbe) so the voltage over resistor 30 is Vreg - (Vb+Vbe) and the current through resistor 30 and transistor 32 is Vreg - (Vb+Vbe) divided by the value of resistor 30. Transistor 32 can be changed by adjusting the value Vb and the only temperature dependence is the Vbe voltage which is easy to compensate by making Vb also temperature dependent.

[0022] The problems with an active biasing circuit such as that of Fig. 3 is that if a battery voltage is used instead of a regulated voltage Vreg, the current is dependent on the battery voltage and also the voltage drop over resistor 30 is usually too high for the power amplifier, which results in increased power loss and lower output power.

[0023] The aforesaid problems associated with the circuits of Figs. 1, 2 and 3 are overcome by the bias control circuit embodiment of the present invention illustrated in Fig. 4.

[0024] Fig. 4 shows a bias circuit for an RF transistor power amplifier 50 including resistors 30, 32, 34, 36, 38, 40 and 42 and transistors 44, 46 and 48. Transistor 44 and resistor 30 form a current generator, the current i1 generated being Ve44 divided by the value R30 of resistor 30. This current flows through resistors 32 and 34 and transistor 46 connected as a diode. The voltage between Vbat and node 52 (V2) is Vbe46 + (i1 x R34) where Vbe46 is the base to emitter voltage of transistor 46 and R34 is the value of resistor 34. An alternative series connection is possible wherein resistor 36 is connected to V_{bat} and transistor 46 is connected to node 52.

[0025] Transistor 48 is part of the bias control circuit for the RF transistor power amplifier 50. The emitter of transistor 48 is connected to the low voltage end of resistor 38 and the drain feeding circuit of transistor power amplifier 50. Resistor 38 functions as a current-to-voltage converter. The collector current of transistor 48 controls the gate voltage of transistor amplifier 50 in such a manner that the voltage drop over resistor 38 is the Vbe voltage of bias control transistor 48 less than the voltage between Vbat and V2, so the voltage drop over resistor 38 is the Vbe46 of transistor 46 + i1 x R34 (the resistance of 34) minus the Vbe48 of transistor 48. A dual transistor is used for transistor diode 46 and bias control transistor 48 so they are quite identical and are both at same temperature. Resistor 36 is used to reject possible RF-frequencies and has almost no voltage drop over it, because only the base current of transistor 48 is flowing through it. Resistor 36 may not be required in all applications. Resistor 42 is dimensioned so that the current through bias control transistor 48 equals i1 at highest power amplifier current. Thus, with highest current level (needed for highest RF power) Vbe voltage of transistors 46 and 48 are equal and cancel each other. The voltage drop over resistor 38 is i1 x R34 and the RF power amplifier current is i1 x R34/R38. Because Vbe of transistors 46 and 48 are cancelled there is no temperature dependence on power amplifier 50 current (i50) and a very small-value for resistor 38 can be used and still the power amplifier current (i50) is exactly controlled with i1. Of course the power amplifier transistor 50 can also be a bipolar device instead of the FET that is shown in Fig. 4.

[0026] The stages 1 and 2 are also controlled with the same current i1. The controlling transistors are 54 and 56. Because the power levels for stages 1 and 2 are smaller, a higher voltage drop over their collector resistors is allowed. An additional voltage drop is affected with resistor 32, (the voltage drop across resistor 32 is i1 x R32). The voltage between Vbat and node 74 is Vbe2 + i1 x R34 + i1 x R32. Resistors 58 and 60 are used for rejecting RF signals and do not affect the DC levels at the bases of transistors 54 and 56. The current through resistor 62 and transistor 64 is [Vbe2 + i1 x (R34 + R32) - Vbe54]/R54 and through stage 2 resistor 66 and transistor 68 is [Vbe2 + i1 x (R34 + R32) - Vbe56]/R66. The currents through transistors 54 and 56 are not the same as through transistor 46 and also their temperatures are different because they are not on the same chip as transistor 46. Because of a higher voltage drop over resistors 62 and 66, a small difference between Vbe54 and Vbe3 or between Vbe2 and Vbe54 has only a minor influence to the currents of transistors 64 and 68. So also these currents are quite accurately controlled with i1.

[0027] The voltage Vbat has no effect on the biasing currents with the circuit of Fig. 4 because the control voltage referred to ground is mirrored to a scaled voltage referred to Vbat. This voltage mirroring is done so that first the control voltage is changed to i1 and this current is again changed to voltage with resistors 34 and 32, but the reference for this new voltage (i1 x (R34 + R32)) is Vbat, and Vbe2 is summed to this mirrored voltage to compensate the temperature dependence of the control transistors base emitter voltage.

[0028] A simple means for the voltage to current conversion with minimal temperature dependence is to use a PNP transistor 70 as an emitter follower and take the base voltage for transistor 44 from the emitter of transistor 68. With this connection the voltage at node 72 (Ve1) is equal with the power level voltage and the current i1 = Ve1/R30 = Vpowerlevel/R30. Of course there are many other possibilities to do the voltage to current conversion.

[0029] Because there is an exact and simple mathematical relationship between power level voltage and the currents for each RF-stage there is no need to adjust the currents in production or if the RF transistor is changed. Instead fixed values for power levels can be used. These can be the same values which are used in the power control loop for different power levels, or these values can be taken from a separate DA converter.

[0030] While a preferred embodiment of the invention

has been disclosed in detail, it should be understood by those skilled in the art that various other modifications may be made to the illustrated embodiment without departing from the scope of the invention as described in the specification and defined in the appended claims.

Claims

1. An RF amplifier circuit comprising a power amplifier stage containing a power transistor (50), a voltage source (Vbat) and biasing means for providing linear operation of said amplifier circuit, where said biasing means comprises a first resistor means (34), which is connected in series with a diode (46), and a current generator circuit (30,44) coupled to a first node (52), for generating a current (i1), **characterised in that:**

   the diode (46) is a transistor, its emitter electrode being coupled to said voltage source (Vbat) and its base and collector electrodes being connected together and coupled through the first resistor means (34) to the first node (52);
   a bias control transistor (48) is provided, its collector electrode being coupled to the control electrode of the power transistor (50), its emitter electrode being coupled to one of the main current conducting electrodes of the power transistor (50) and its base electrode being coupled to the first node (52) so that the bias control transistor (48) is responsive to the voltage at first node (52) and provides a bias control current signal to said power transistor (50); and
   a current-to-voltage converter means (38) is connected between the emitter electrode of said bias control transistor (48) and said voltage source (Vbat);

   wherein the base-to-emitter voltages of said transistor diode (46) and said bias control transistor (48) are determined by the generated current (i1) to be substantially equal, the transistor diode (46) and bias control transistor (48) being identical transistors maintained at equal temperatures.

2. An RF amplifier circuit according to claim 1 further including a second resistor means (36) connected between said bias control transistor (48) and said first node (52).

3. An RF amplifier circuit according to claim 1 or 2, wherein said current-to-voltage converter means (38) is a resistor means.

4. An RF amplifier circuit according to any of claims 1 to 3, further including a series resistor means (40, 42) connected to said bias control transistor (48) and to said power transistor (50).

5. An RF amplifier circuit according to any of claims 1 to 4, further including a first and second transistor amplifier stage wherein said first transistor amplifier stage includes a transistor (64) and said second transistor amplifier stage includes a transistor (68), wherein said biasing means comprises a bias control transistor (54) connected between said transistor (64) of the first transistor amplifier stage and said current generator circuit and a bias control transistor (56) connected between said transistor (68) of said second transistor amplifier stage and said current generator.

6. An RF amplifier circuit according to claim 5, wherein said bias control transistor (54) of said first transistor amplifier stage includes an emitter, a collector and a base electrode, said bias control transistor (56) of said second transistor amplifier includes an emitter, a collector and a base electrode and wherein said current generator circuit is connected to said base electrodes of said bias control transistors (54, 56) of said first and second transistor amplifier stages, wherein said current generator circuit is connected to said first node (52) through a second resistor means (32) and wherein said second resistor means (32) and said bias control transistors (54, 56) of the first and second transistor amplifier stages are connected to said current generator circuit at a second node (74).

7. An RF amplifier circuit according to claim 5 or 6, wherein said voltage source (Vbat) is connected to said bias control transistors (54, 56) of said first and second amplifier stages by second and third bias control resistor means (62, 66) respectively.

8. An RF amplifier circuit according to any of claims 1 to 7, wherein said current generator circuit includes a transistor (44) connected in series with a resistor (30) and a power input signal connected to said transistor (44) to provide said generated current (i1).

9. An RF amplifier circuit according to claim 8, wherein said transistor (44) of said current generator circuit includes a base, and emitter and a collector electrode, said emitter electrode being connected to said resistor (30) and wherein said current generator circuit further includes a PNP transistor (70), having a base electrode connected to a power level input signal, an emitter electrode connected to said base electrode of said transistors (44) and through a resistor (76) to a source of regulating voltage (Vreg).

10. An RF amplifier circuit according to claim 9, wherein said collector of said PNP transistor (70) and said resistor (30) are connected to a source of ground voltage and wherein said series resistor means (40, 42) is connected to a source of negative voltage.

11. An RF amplifier circuit according to any of claims 1 to 10, wherein said transistor diode (46) has its said emitter electrode connected to said voltage source (Vbat) and its said base and collector electrodes connected to said first resistor means (34), and wherein said bias control transistor (48) has its said emitter electrode connected to said current-to-voltage converter means (38), its said collector electrode connected to said series resistor means (40, 42) and its said base electrode connected to said node (52).

12. An RF amplifier circuit according to any of claims 1 to 11, wherein the voltage drop over said current-to-voltage converter (38) is substantially equal to the base-to-emitter voltage of said transistor diode (46) plus the value of the current from said current generator times the value of first resistor means (34) minus the base-to-emitter voltage of said bias control transistor.

Patentansprüche

1. HF-Verstärkerschaltkreis, der eine Leistungsverstärkerstufe umfasst, die einen Leistungstransistor (50), eine Spannungsquelle (Vbat) und ein Vorspannmittel zum Bereitstellen eines linearen Betriebs des Verstärkerschaltkreises enthält, wobei das Vorspannmittel ein erstes Widerstandsmittel (34), das in Serie mit einer Diode (46) geschaltet ist, und einen Stromerzeugerschaltkreis (30, 44) umfasst, der an einen ersten Knoten (52) gekoppelt ist, um einen Strom (i1) zu erzeugen,
dadurch gekennzeichnet, dass:

- die Diode (46) ein Transistor ist, wobei seine Emitterelektrode an die Spannungsquelle (Vbat) gekoppelt ist und seine Basis- und Kollektorelektroden verbunden sind, wobei der Serienschaltkreis, der durch die Diode (46) und das erste Widerstandsmittel (34) gebildet wird, zwischen die Spannungsquelle (Vbat) und den ersten Knoten (52) geschaltet ist, wobei entweder die Diode (46) oder das erste Widerstandsmittel (34) mit dem ersten Knoten (52) verbunden ist;
- ein Vorspannungs-Steuertransistor (48) bereitgestellt wird, wobei seine Kollektorelektrode an die Steuerelektrode des Leistungstransistors (50) gekoppelt ist, wobei seine Emitterelektrode an eine der Hauptstrom-führenden Elektroden des Leistungstransistors (50) gekoppelt ist und seine Basiselektrode an den ersten Knoten (52) gekoppelt ist, so dass der Vorspannungs-Steuertransistor (48) auf die Spannung an dem ersten Knoten (52) anspricht und ein Vorspannungs-Steuerstrom-Signal dem Leistungstransistor (50) bereitstellt; und
- ein Strom-Zu-Spannungs-Konverter-Mittel (38) zwischen die Emitterelektrode des Vorspannungs-Steuertransistors (48) und der Spannungsquelle (Vbat) geschaltet ist;

wobei die Basis-Zu-Emitter-Spannungen der Transistordiode (46) und des Vorspannungs-Steuertransistors (48) durch den erzeugten Strom (i1) derart bestimmt sind, dass sie im wesentlichen gleich sind, wobei die Transistordiode (46) und der Vorspannungs-Steuertransistor (48) identische Transistoren sind, die auf gleichen Temperaturen gehalten werden.

2. HF-Verstärkerschaltkreis gemäß Anspruch 1, der ferner ein zweites Widerstandsmittel (36) einschließt, das zwischen dem Vorspannungs-Steuertransistor (48) und dem ersten Knoten (52) geschaltet ist.

3. HF-Verstärkerschaltkreis gemäß Anspruch 1 oder 2, wobei das Strom-Zu-Spannungs-Konverter-Mittel (38) ein Widerstandsmittel ist.

4. HF-Verstärkerschaltkreis gemäß einem der Ansprüche 1 bis 3, der ferner ein Serienwiderstandsmittel (40, 42) einschließt, das mit dem Vorspannungs-Steuertransistor (48) und dem Leistungstransistor (50) verbunden ist.

5. HF-Verstärkerschaltkreis gemäß einem der Ansprüche 1 bis 4, der ferner eine erste und zweite Transistorverstärkerstufe einschließt, wobei die erste Transistorverstärkerstufe einen Transistor (64) einschließt und die zweite Transistorverstärkerstufe einen Transistor (68) einschließt, wobei -das Vorspannmittel einen Vorspannungs-Steuertransistor (54), der zwischen dem Transistor (64) der ersten Transistorverstärkerstufe und dem Stromerzeugerschaltkreis geschaltet ist, und einen Vorspannungs-Steuertransistor (56) umfasst, der zwischen den Transistor (68) der zweiten Transistorverstärkerstufe und dem Stromerzeuger geschaltet ist.

6. HF-Verstärkerschaltkreis gemäß Anspruch 5, wobei der Vorspannungs-Steuertransistor (54) der ersten Transistorverstärkerstufe eine Emitter-, eine Kollektor- und eine Basiselektrode einschließt, wobei der Vorspannungs-Steuertransistor (56) des zweiten Transistorverstärkers eine Emitter-, eine Kollektor- und eine Basiselektrode einschließt und

wobei der Stromerzeugerschaltkreis mit der Basiselektrode der Vorspannungs-Steuertransistoren (54, 56) der ersten und der zweiten Transistorverstärkerstufe verbunden ist, wobei der Stromerzeuger-Schaltkreis mit dem ersten Knoten (52) durch ein zweites Widerstandsmittel (32) verbunden ist und wobei das zweite Widerstandsmittel (32) und die Vorspannungs-Steuertransistoren (54, 56) der ersten und der zweiten Transistorverstärkerstufe mit dem Stromerzeugerschaltkreis an einem zweiten Knoten (74) verbunden sind.

7. HF-Verstärkerschaltkreis gemäß Anspruch 5 oder 6, wobei die Spannungsquelle (Vbat) mit den Vorspannungs-Steuertransistoren (54, 56) der ersten und zweiten Verstärkerstufe durch zweite bzw. dritte Vorspannungs-Steuerwiderstandsmittel (62, 66) verbunden sind.

8. HF-Verstärkerschaltkreis gemäß einem der Ansprüche 1 bis 7, wobei der Stromerzeugerschaltkreis einen Transistor (44), der mit einem Widerstand (30) in Reihe geschaltet ist, und ein Leistungs-Eingangssignal einschließt, das mit dem Transistor (44) verbunden ist, um den erzeugten Strom (i1) bereitzustellen.

9. HF-Verstärkerschaltkreis gemäß Anspruch 8, wobei der Transistor (44) des Stromerzeugerschaltkreises eine Basis-, eine Emitter- und eine Kollektorelektrode einschließt, wobei die Emitterelektrode mit dem Widerstand (30) verbunden ist und wobei der Stromerzeugerschaltkreis einen PNP Transistor (70), der eine Basiselektrode aufweist, die mit einem Leistungspegel-Eingangssignal verbunden ist, und eine Emitterelektrode einschließt, die mit der Basiselektrode des Transistors (44) und durch einen Widerstand (76) mit einer Regelspannungs-Quelle (Vreg) verbunden ist.

10. HF-Verstärkerschaltkreis gemäß Anspruch 9, wobei der Kollektor des PNP Transistors (70) und der Widerstand (30) mit einer Erdspannungs-Quelle verbunden sind und wobei das Serienwiderstandsmittel (40, 42) mit einer Quelle negativer Spannung verbunden ist.

11. HF-Verstärkerschaltkreis gemäß einem der Ansprüche 1 bis 10, wobei die Emitterelektrode der Transistordiode (46) mit der Spannungsquelle (Vbat) verbunden ist und die Basis- und Kollektorelektrode mit dem ersten Widerstandsmittel (34) verbunden sind und wobei die Emitterelektrode des Vorspannungs-Steuertransistors (48) mit dem Strom-Zu-Spannungs-Konverter-Mittel (38) verbunden ist und die Kollektorelektrode mit dem Serienwiderstandsmittel (40, 42) verbunden ist und die Basiselektrode mit dem Knoten (52) verbunden ist.

12. HF-Verstärkerschaltkreis gemäß einem der Ansprüche 1 bis 11, wobei der Spannungsabfall über den Strom-Zu-Spannungs-Konverter (38) im wesentlichen gleich der Basis-Zu-Emitter-Spannung der Transistordiode (46) plus dem Wert des Stroms von dem Stromerzeuger mal dem Wert des ersten Widerstandsmittels (34) minus der Basis-Zu-Emitter-Spannung des Vorspannungs-Steuertransistors ist.

Revendications

1. Circuit amplificateur radiofrèquence comprenant un étage amplificateur de puissance contenant un transistor de puissance (50), une source de tension (Vbat) et des moyens de polarisation pour obtenir un fonctionnement linéaire dudit circuit amplificateur, dans lequel lesdits moyens de polarisation comprennent des premiers moyens de résistance (34), qui sont connectés en série à une diode (46), et un circuit générateur de courant (30, 44) couplé à un premier noeud (52), pour générer un courant (i1), **caractérisé en ce que** :

   la diode (46) est un transistor, son électrode d'émetteur étant couplée à ladite source de tension (Vbat) et ses électrodes de base et de collecteur étant connectées l'une à l'autre, le circuit série formé par ladite diode (46) et lesdits premiers moyens de résistance (34) étant connecté entre ladite source de tension (Vbat) et ledit premier noeud (52), la diode (46) ou les premiers moyens de résistance (34) étant connectés audit premier noeud (52) ;
   un transistor de commande de polarisation (48) est prévu, son électrode de collecteur étant couplée à l'électrode de commande du transistor de puissance (50), son électrode d'émetteur étant couplée à l'une des électrodes de conduction de courant principal du transistor de puissance (50) et son électrode de base étant couplée au premier noeud (52) de sorte que le transistor de commande de polarisation (48) soit sensible à la tension au niveau du premier noeud (52) et délivre un signal de courant de commande de polarisation audit transistor de puissance (50) ; et
   des moyens de conversion courant-tension (38) sont connectés entre l'électrode d'émetteur dudit transistor de commande de polarisation (48) et ladite source de tension (Vbat) ;

   dans lequel les tensions base-émetteur de ladite diode de transistor (46) et dudit transistor de commande de polarisation (48) sont déterminées

par le courant généré (i1) de manière à être sensiblement égales, la diode de transistor (46) et le transistor de commande de polarisation (48) étant des transistors identiques maintenus à des températures égales.

2. Circuit amplificateur radiofréquence selon la revendication 1, comprenant en outre des deuxièmes moyens de résistance (36) connectés entre ledit transistor de commande de polarisation (48) et ledit premier noeud (52).

3. Circuit amplificateur radiofréquence selon la revendication 1 ou 2, dans lequel lesdits moyens de conversion courant-tension (38) sont des moyens de résistance.

4. Circuit amplificateur radiofréquence selon l'une quelconque des revendications 1 à 3, comprenant en outre des moyens de résistance série (40, 42) connectés audit transistor de commande de polarisation (48) et audit transistor de puissance (50).

5. Circuit amplificateur radiofréquence selon l'une quelconque des revendications 1 à 4, comprenant en outre des premier et deuxième étages amplificateurs à transistors, dans lequel ledit premier étage amplificateur à transistor comprend un transistor (64) et ledit deuxième étage amplificateur à transistor comprend un transistor (68), dans lequel lesdits moyens de polarisation comprennent un transistor de commande de polarisation (54) connecté entre ledit transistor (64) du premier étage amplificateur à transistor et ledit circuit générateur de courant et un transistor de commande de polarisation (56) connecté entre ledit transistor (68) dudit deuxième étage amplificateur à transistor et ledit générateur de courant.

6. Circuit amplificateur radiofréquence selon la revendication 5, dans lequel ledit transistor de commande de polarisation (54) dudit premier étage amplificateur à transistor comprend des électrodes d'émetteur, de collecteur et de base, ledit transistor de commande de polarisation (56) dudit deuxième amplificateur à transistor comprend des électrodes d'émetteur, de collecteur et de base, et dans lequel ledit circuit générateur de courant est connecté auxdites électrodes de base desdits transistors de commande de polarisation (54, 56) desdits premier et deuxième étages amplificateurs à transistors, dans lequel ledit circuit générateur de courant est connecté audit premier noeud (52) par l'intermédiaire de deuxièmes moyens de résistance (32), et dans lequel lesdits deuxièmes moyens de résistance (32) et lesdits transistors de commande de polarisation (54, 56) des premier et deuxième étages amplificateurs à transistors sont connectés audit circuit générateur de courant au niveau d'un deuxième noeud (74).

7. Circuit amplificateur radiofréquence selon la revendication 5 ou 6, dans lequel ladite source de tension (Vbat) est connectée auxdits transistors de commande de polarisation (54, 56) desdits premier et deuxième étages amplificateurs, respectivement, par des deuxièmes et troisièmes moyens de résistance de commande de polarisation (62, 66).

8. Circuit amplificateur radiofréquence selon l'une quelconque des revendications 1 à 7, dans lequel ledit circuit générateur de courant comprend un transistor (44) connecté en série à une résistance (30) et un signal d'entrée de puissance connecté audit transistor (44) afin de fournir ledit courant généré (i1).

9. Circuit amplificateur radiofréquence selon la revendication 8, dans lequel ledit transistor (44) dudit circuit générateur de courant comprend des électrodes de base, d'émetteur et de collecteur, ladite électrode d'émetteur étant connectée à ladite résistance (30), et dans lequel ledit circuit générateur de courant comprend, en outre, un transistor PNP (70), ayant une électrode de base connectée à un signal d'entrée de niveau de puissance, une électrode d'émetteur connectée à ladite électrode de base dudit transistor (44) et par l'intermédiaire d'une résistance (76) à une source de tension de régulation (Vreg).

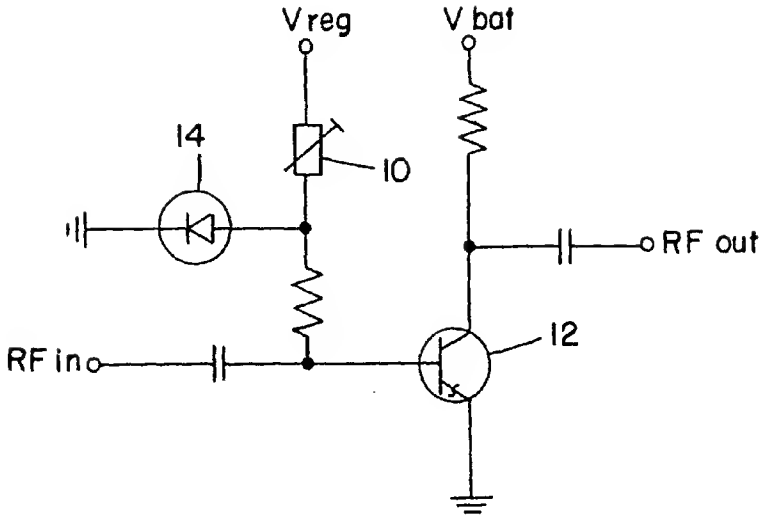
10. Circuit amplificateur radiofréquence selon la revendication 9, dans lequel ledit collecteur dudit transistor PNP (70) et ladite résistance (30) sont connectés à une source de tension de masse, et dans lequel lesdits moyens de résistance série (40, 42) sont connectés à une source de tension négative.

11. Circuit amplificateur radiofréquence selon l'une quelconque des revendications 1 à 10, dans lequel ladite diode de transistor (46) a sa dite électrode d'émetteur connectée à ladite source de tension (Vbat) et ses dites électrodes de base et de collecteur connectées auxdits premiers moyens de résistance (34), et dans lequel ledit transistor de commande de polarisation (48) a sa dite électrode d'émetteur connectée auxdits moyens de conversion courant-tension (38), sa dite électrode de collecteur connectée auxdits moyens de résistance série (40, 42) et sa dite électrode de base connectée audit noeud (52).

12. Circuit amplificateur radiofréquence selon l'une quelconque des revendications 1 à 11, dans lequel la chute de tension sur ledit convertisseur courant-tension (38) est sensiblement égale à la tension ba-

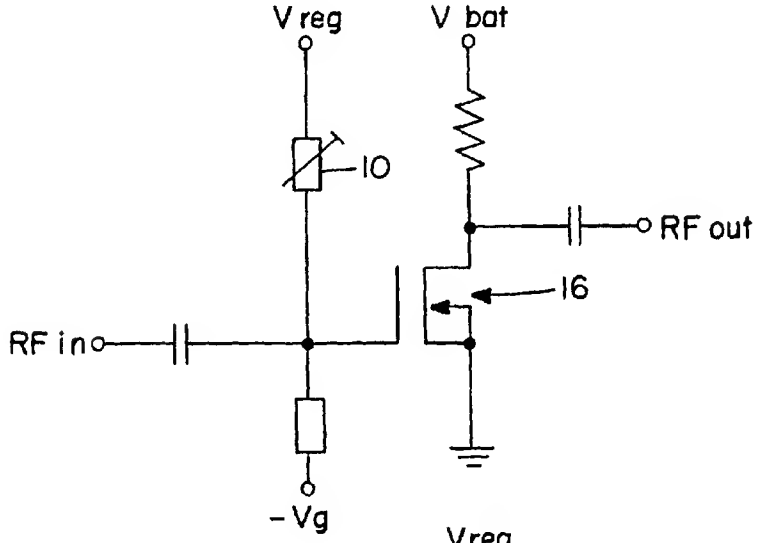
se-émetteur de ladite diode de transistor (46) plus la valeur du courant provenant dudit générateur de courant multipliée par la valeur des premiers moyens de résistance (34) moins la tension base-émetteur dudit transistor de commande de polarisation.

FIG. 1.



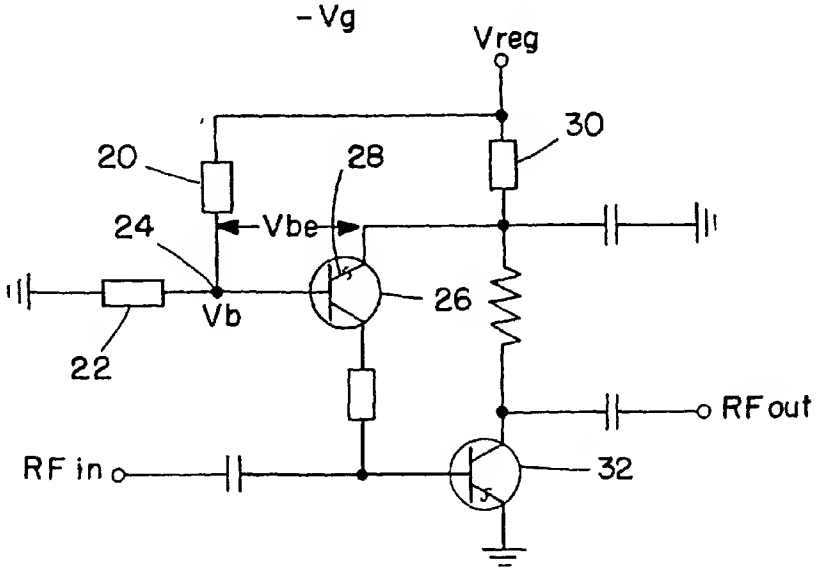
PRIOR ART

FIG. 2.



PRIOR ART

FIG. 3.



PRIOR ART

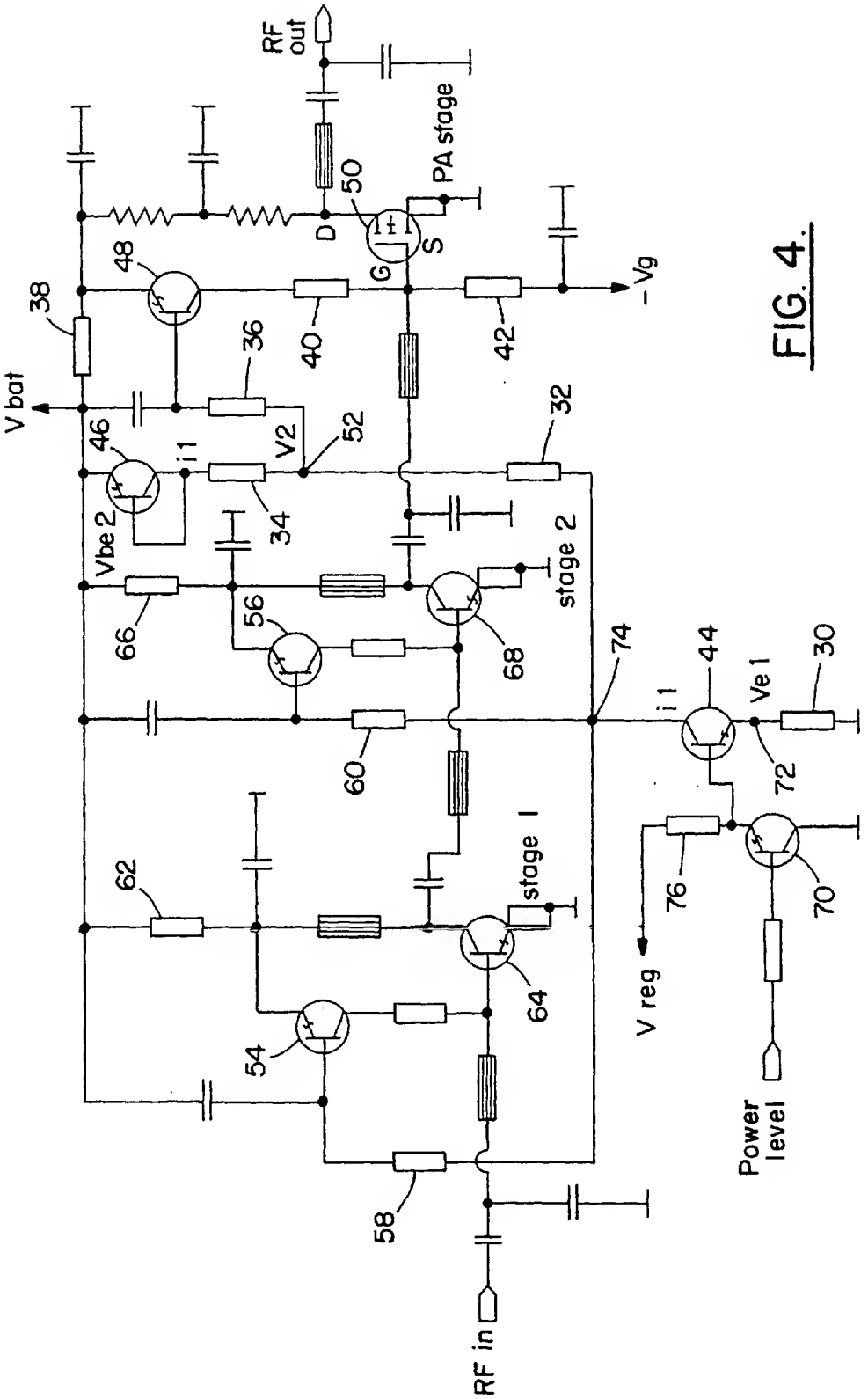

RF out
PA stage
50
D
G
S
48
38
36
40
42
-Vg
V bat
46
i1
V2
52
32
34
Vbe 2
stage 2
66
56
68
74
44
i1
Ve 1
30
60
72
62
stage 1
64
76
70
V reg
54
Power level
58
RF in

FIG. 4.